REMARKS

Claims 1 - 20 are all the claims presently pending in the application. Claims 7-20 have added. Claims 1 and 10 are independent.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "**Version with markings to show changes made.**" These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicants also note that, notwithstanding any claim amendments herein or later during prosecution, that Applicants' intent is to encompass equivalents of all claim elements.

Claims 1-6 stand rejected under 35 U.S.C. § 112, second paragraph as indefinite. Claims 4-6 stand rejected under 35 U.S.C. § 112, first paragraph as containing subject matter not described in the specification. Claims 1-2 stand rejected under 35 U.S.C. § 102(b) as anticipated by Kodate et al. (U.S. Pat. 5,521,728).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a device for a display system including an array of pixel cells formed on a substrate wherein each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. The device includes a first and second transistor formed on the

substrate each having a gate electrode and first and second electrodes defining a serpentine channel region there between, whereby voltage applied to the gate electrode controls conductivity of the channel region.

Conventional display systems include pixel cells formed on a substrate which are each coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one date line of a plurality of data lines formed on the substrate. An array tester provides a means for testing the cells of such a display system by coupling probes to gate line pads and data line pads that terminate the gate lines and data lines, respectively. In other words, the array tester is coupled directly to each gate line and each data line. However, when the size of such a conventional display system is changed the spacing of the gate lines and/or data lines also changes which requires that the probe fixture of the array tester be modified to accommodate these changes.

By contrast, the present invention includes first and second electrodes (e.g., in addition to the pixel array) which accommodate variations in size and/or resolution without requiring modification of the probe fixture of the array tester. In other words, the present invention provides a flexible interface between the array under test and the test system. More specifically, in the event that the size of the array under test is changed, the gate line select/hold circuit 17 and/or the data line select/hold circuit 19 and the probe pads associated therewith may be designed such that they align with the spacing of an existing probe fixture, thereby eliminating the high costs associated with redesigning the probe fixture of the array.

Further, each of the first and second transistors have a gate electrode and first and second

electrodes defining a serpentine channel region there between. This feature minimizes the time constant required to transfer a charge to/from a capacitive load using the select and hold transistors of the gate line select/hold circuit 17 and the data line select/hold circuit 19 and also reduces the ON resistance of these transistors. The ON resistance of the transistor is proportional to the channel length/width ratio of the transistor. The serpentine channel region minimizes this length/width ratio and, therefore, reduces the ON resistance and the time constant.

II. THE 35 U.S.C. § 112, SECOND PARAGRAPH REJECTION

The Examiner alleges that claims 1-6 are indefinite. Applicant submits, however, that these claims particularly point out and distinctly claim the subject matter regarded as the invention.

Specifically, the Office Action alleges that it is unclear what "a first and second transistor" represent. However, Applicants respectfully submit that the first and second transistors are clearly shown in, for example, Fig. 8 as 801 and 803, for the gate lines and in Fig. 9 as 901 and 903 for the data lines, respectively. Applicants respectfully request withdrawal of this rejection.

III. THE 35 U.S.C. § 112, FIRST PARAGRAPH REJECTION

The Examiner alleges that claims 4-6 contain subject matter which was not described in the specification in such a way as to enable one of ordinary skill in the art to practice the invention. Specifically, the Examiner alleges that the specification does not disclose the first transistor coupled between a data line and a probe pad as recited in claim 4, a second transistor

coupled between a gate line and a probe pad as recited in claim 5 and a second transistor coupled between a data line and a probe pad as recited in claim 6. However, as explained above, Applicants respectfully submit that the first and second transistors are clearly shown in, for example, Fig. 8 as 801 and 803, for the gate lines and in Fig. 9 as 901 and 903 for the data lines, respectively. Applicants respectfully request withdrawal of this rejection.

IV. THE PRIOR ART REJECTION

The Examiner alleges that the Kodate et al. reference teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by these references.

The Kodate et al. reference discloses a circuit (as shown in Fig. 6) having a plurality of pixel cells 36 formed on a substrate and connected to a plurality of data lines 10 and a plurality of gate lines 24. However, this is a very generic description of an active matrix display. While Applicants agree that the Kodate et al. reference appears to disclose a first transistor 38, the Kodate et al. reference does not teach or suggest a second transistor as recited in independent claim 1.

The Kodate et al. reference also does not teach or suggest first and second electrodes defining a serpentine channel region. In fact, the Kodate et al. reference discloses a completely different shape. The Kodate et al. reference states "as shown in Fig. 4, each gate line 24 . . . at a little angle with the width direction of the frame area 1, and thus, the shape of the blocking layers 26 and 30 is parallelogram of trapezoid" (col. 7, lines 42-50). Therefore, the Kodate et al.

reference specifically teaches a parallelogram of a trapezoid and not a serpentine channel region. The Kodate et al. reference states again "as shown in Fig. 2, since the individual data lines 10 are extending in the frame area 1 toward the peripheral portion . . . so that the spacing between them become narrower, the blocking layer 12 is shaped in a parallelogram of a trapezoid, . . . each gate line 24 . . . at a little angle with the width direction of the frame area 1, and thus, the shape of the blocking layers 26 and 30 is a parallelogram of trapezoid" (col. 6, lines 15-25). Therefore, the Kodate et al. reference does not teach or suggest first and second electrodes defining a serpentine channel region.

Further, those of ordinary skill in the art recognize that the active matrix gate and data line fanouts of the Kodate et al. reference are formed to allow only a parallelogram of trapezoid shape between the gate and data lines and do not teach or suggest a serpentine structure. Clearly, the parallelogram of a trapezoid disclosed by the Kodate et al. reference in, for example, Fig. 4 is in stark contrast to the serpentine shape of the present invention as shown, for example, in Fig. 10B.

Additionally, the Kodate et al. reference only discloses a single transistor 38 between the gate or data lines of the array. In contrast, the present invention recites a first and second transistor. As shown in Fig. 8 and 9, respectively, that includes either a first (801) and second (803) transistor or of a first (901) and second transistor (903). Specifically, page 19, lines 10 through 14 of the present specification teaches "the gate line select/hold circuitry . . . includes at least one select transistor . . and at least one hold transistor . . . corresponding to each gate line in the group." The Kodate et al. reference does not teach or suggest a second transistor.

Moreover, regarding claim 2, the Kodate et al. reference discloses that the single transistor 38 is connected to two, and only two, data lines (or two gate lines). The Kodate et al. reference discloses that the transistor 30 "is connected to two data lines 10 functioning as a source electrode and a drain electrode . . . this transistor is repeatedly formed . . " The Kodate et al. reference does not teach or suggest a common electrode comprises one of the first and second electrodes of the first transistor and one of the first and second electrodes of the second transistor as recited by claim 2.

Further, the Kodate et al. reference does not address the problem solved by the present invention. Rather, the Kodate et al. reference teaches a display device that allegedly solves three problems: 1) light blocking ability of the frame area; 2) preventing electrostatic failure; and 3) without increasing manufacturing processes (col. 3, lines 32-45). The Kodate et al. reference does not mention and has no intention of using the display device in any sort of testing. By contrast, the present invention among other things, solves the "the need in the art for an array test system whereby the configuration of the array test system can be changed with minimal cost in order to accommodate variations in the size and/or resolution of the TFT/LCD display array under test" (page 1, lines 22-24).

Lastly, the system disclosed by the Kodate et al. reference operates quite differently than the device of the present invention. For example, the Kodate et al. reference teaches that "each data (or gate line) 10 is connected to the source/drain electrode of the transistor 38 formed between the lines 10", thus having two common nodes with the lines, but also that "the gate electrode of the transistor 38 is capacitive-coupled to the data lines", and further, "on both sides"

(col. 9, lines 36-45). By contrast, with respect to claim 2, the present invention may have one common electrode with the lines. Additionally, in one exemplary embodiment, the "select logic for the group is controlled by control signals supplied to the select logic via data select control pads through direct signal contact to the gate electrode" (page 5, lines 21-22).

Therefore, contrary to the allegations of the Examiner, the Kodate et al. reference does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

V. FORMAL MATTERS AND CONCLUSION

The Office Action objects to the title of the invention. This Amendment amends the title to read: "INTEGRATED CIRCUITS FOR TESTING AN ACTIVE MATRIX DISPLAY ARRAY". Applicants respectfully request withdrawal of this objection.

The Office Action objects to the abstract of the disclosure. This Amendment amends the abstract in accordance with Examiner Nguyen's helpful suggestion. Applicants respectfully request withdrawal of this objection.

The Office Action objects to the drawings. This Amendment encloses a Submission of Proposed Drawing Corrections which corrects Figures 2 and 3 to add legends in accordance with Examiner Nguyen's helpful suggestion. Applicants respectfully request withdrawal of this objection.

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-20, all the claims presently pending in the Application, are patentably distinct over the

prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT:

A device for use in a display system [comprising] including an array of pixel cells formed on a substrate. Each pixel cell [is] being coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines being formed on the substrate. The device [comprises] includes first and second transistors formed on [said] the substrate. Each transistor has a gate electrode and first and second electrodes defining a serpentine channel region there between [Voltage] voltage applied to the gate electrode controls conductivity of the channel region. Preferably, [the] a common electrode [comprises] includes one of the first and second electrodes of [said] the first transistor and one of [said] the first and second electrodes of [said] the second transistor. The first and second transistors are preferably coupled between a gate line (or data line) and respective probe pads formed on the substrate and selectively couple the respective probe pad to the gate line (or data line) during a test routine whereby charge is written to, stored, and read from the array of pixel cells.

IN THE CLAIMS:

Please add claims 7 - 20 as follows:

- - 7. (Newly Added) The system of claim 1, wherein said first transistor comprises a select transistor and is connected to a first probe pad and a gate select control pad and wherein said second transistor comprises a hold transistor and is connected to a second probe pad and a gate hold control pad. - -

- - 8. (Newly Added) The system of claim 7, wherein said select transistor and said hold transistor are connected by a common electrode to at least one of said plurality of gate lines. - -

- - 9. (Newly Added) The system of claim 7, wherein said select transistor and said hold transistor are connected to by a common electrode to at least one of said plurality of data lines. - -

- - 10. (Newly Added) A display system comprising:

an array of pixel cells formed on a substrate, wherein each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate;

a gate line select/hold circuit formed on said substrate and connected to at least one of said plurality of gate lines, a first control pad and a first probe pad; and

a data line select/hold circuit formed on said substrate and connected to at least one of said plurality of data lines, a second control pad and a second probe pad, wherein at least one of the gate line select/hold circuit and the data line select/hold circuit comprises first and second transistors each having first and second electrodes defining a serpentine channel region. - -

- - 11. (Newly Added) The system of claim 10, wherein said gate line select/hold circuit is connected to a set of said plurality of gate lines. - -

- - 12. (Newly Added) The system of claim 10, wherein said data line select/hold circuit is

connected to a set of said plurality of data lines. - -

- - 13. (Newly Added) The system of claim 10, wherein said gate line select/hold circuit is connected to a plurality of first control pads. - -

- - 14. (Newly Added) The system of claim 10, wherein said data line select/hold circuit is connected to a plurality of second control pads. - -

- - 15. (Newly Added) The system of claim 10, wherein said gate line select/hold circuit includes a select logic and a hold logic. - -

- - 16. (Newly Added) The system of claim 10, wherein said data line select/hold circuit includes a select logic and a hold logic. - -

- - 17. (Newly Added) The system of claim 10, wherein said gate line select/hold circuit is connected to a third probe pad and third control pad. - -

- - 18. (Newly Added) The system of claim 17, wherein said gate line select/hold circuit comprises:

a select logic connected to said first probe pad and to a plurality of said first control pads; and

a hold logic connected to said third probe pad and to a plurality of said third control pads.

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- - 19. (Newly Added) The system of claim 10, wherein said data line select/hold circuit is connected to a third probe pad and third control pad. - -

- - 20. (Newly Added) The system of claim 19, wherein said data line select/hold circuit comprises:

a select logic connected to said second probe pad and to a plurality of said second control pads; and

a hold logic connected to said third probe pad and to a plurality of said third control pads.

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